SpW-10X Router ASIC Testing And Performance

Session: SpaceWire Components

Short Paper

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ABSTRACT

The SpW-10X SpaceWire routing switch ASIC is a radiation tolerant device with eight SpaceWire ports and two parallel ports. It supports both path and logical addressing, includes various failure detection and power saving features, operates at up to 200 Mbits/s and switches packets in less than 0.5 µs. LVDS drivers and receivers are included on-chip to save board area, mass and power.

The SpW-10X device is now being sold by Atmel as the AT7910E and is being designed into space missions. This paper introduces the SpW-10X device, describes how it was tested and summarises its performance characteristics.

1 SpW-10X overview

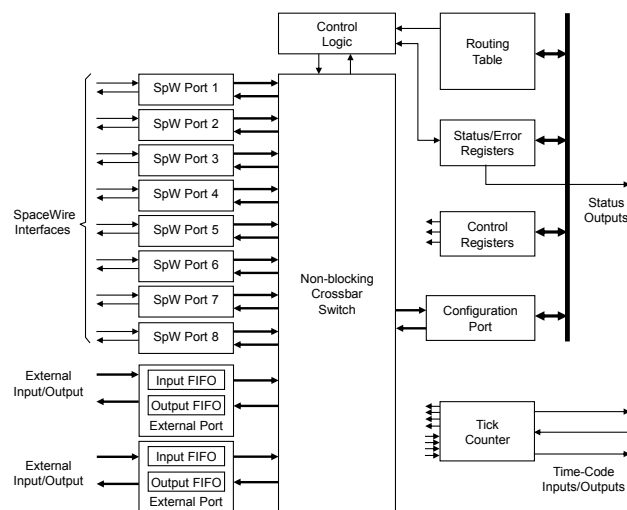The SpaceWire routing switch is a key element in any SpaceWire network [1].

Figure 1 SpW-10X SpaceWire Routing Switch

The SpW-10X routing switch IP core was designed for ESA by University of Dundee and Austrian Aerospace, validated by EADS Astrium GmbH and manufactured by Atmel. It is now available as a radiation tolerant ASIC from Atmel (part no. AT7910E) [2]. The architecture of the SpW-10X is illustrated in Figure 1.

It has the following main features:

- Eight SpaceWire ports.
- Two external parallel ports, each comprising an input FIFO and an output FIFO.
- A non-blocking crossbar switch connecting any input port to any output port.
- An internal configuration port accessible via the crossbar switch from the external parallel ports or the SpaceWire ports.
- A routing table accessible via the configuration port which holds the logical address to output port mapping.
- Logic to control the operation of the switch, performing arbitration and group adaptive routing.
- Control registers that can be written and read by the configuration port using the RMAP protocol [3] and which hold control information e.g. link operating speed.
- An external time-code interface used for sending and receiving time or synchronisation information over a SpaceWire network.
- Watchdog timers on all ports.
- External status/error signals.
- Supports both path and logical addressing.
- Provides priority routing based on logical address.
- Supports group adaptive routing.
- Includes several power saving features to reduce overall power consumption.
- Provides 'disable on silence' and 'start on request' capability.
- Implemented in 0.35µm MH1RT radiation tolerant technology from ATMEL.
- Radiation tolerant: total dose 300Krad(Si), no latchup up to 70 MeV/mg/cm^2.

2   SPW-10X VERIFICATION, VALIDATION AND CHARACTERISATION

The SpW-10X device has been tested in several different ways:

- During design by University of Dundee a VHDL tests bench was used for initial testing.
- An independent test bench was developed by Austrian Aerospace providing extensive tests and identifying several issues with the initial VHDL code.
- The Router IP was implemented in several STAR-Dundee devices and has been widely used by many organisations.
- The SpW-10X device was implemented in a Xilinx FPGA with the design kept as close as possible to the final VHDL code used for the ASIC design. This SpW-10X FPGA was extensively tested by EADS Astrium GmbH.

- A second SpW-10X FPGA device was implemented as a mezzanine board in preparation for final ASIC prototype testing.
- A similar board was designed to carry the SpW-10X ASIC. As soon as the SpW-10X device was available it was mounted on this test board.

The prototype ASIC devices were delivered in November 2007 and an extensive test campaign was then performed to fully characterise the devices:

- Functional validation by EADS Astrium,
- Performance testing by University of Dundee,
- Characterisation by Austrian Aerospace.

3 VERIFICATION

The verification of the SpW-10X is based on the following cornerstones:

- VHDL Testbench with self-checking scenarios
- RTL and Netlist (FPGA and ASIC) verified with the test bench
- Code coverage checked for RTL simulations
- Analysis of requirements which were not possible to simulate
- Timing of ASIC verified with static timing analysis

The verification of the SpW-10X started in parallel to the VHDL development of the SpaceWire Router and was used continuously to debug the design. The formal verification was run with the final FPGA RTL design, FPGA netlist, ASIC RTL design and ASIC netlist. The results are:

- All functions have been checked and show that there are no errors
- Simulation and analysis have been used for the verification
- FPGA and ASIC netlist verification showed that the implementation is correct

4 SpW-10X VALIDATION

Validation was performed against the SpW-10X Specification checking first the FPGA implementation and then the ASIC against each of the requirements in the specification. All the validation tests were performed successfully. There were two clarifications required during FPGA testing: path addressing with different priority levels was not required and the exact value for the Output Port Timeout Interval was specified. During ASIC testing a clarification was made by Atmel that the LVDS I/O cells perform disable rather than tri-state.

5 SpW-10X NETWORK TESTING

Extensive testing of the SpW-10X ASIC in various network configurations was carried out by University of Dundee. No anomalies were found in the ASIC device.

6 SpW-10X Characterisation

Austrian Aerospace performed extensive characterisation of the SpW-10X ASIC device including supply voltage, temperature and power consumption measurements. A summary of the results of these tests are provided below:

- SpW data rate configurable up to 200Mbps
- Single supply voltage of 3.3V (3.0 to 3.6V)
- Temperature:
    - Operational ambient temperature -55°C to +125°C
    - Maximum junction temperature +175°C
    - Maximum lead temperature (soldering 10 sec) +300°C
    - Storage temperature -65°C to +150°C
- Radiation
    - Total dose 300Krad(Si)
    - No latchup up to 70 MeV/mg/cm^2
    - Package MQFP 196 with 25 mil pin spacing
- Power consumption (max):
    - Static Pst: 1W
    - OFF condition Poff: 1.6W
    - Total operational all SpW IF active Pop:
      3.7W @ 200Mbps, 3.0W @ 100Mbps, 2.4W @ 10Mbps
    - Deactivated (Clk and LVDS buffer) SpW link: reduction of power by (Pop - Poff) × 0.1 + 0.06; E.g. with two SpW links deactivated operating at 200Mbps the power consumption is 3.16W
    - Data flow has very little influence on power consumption
    - For lower supply voltage (<3.6V):
      resistive model can be used, e.g. 69.4% of power at 3.0V

7 Summary

The SpW-10X ASIC operates at up to 200 Mbits/s on all links. Packet switching times are approximately 0.5 μs with a maximum latency of 0.55 μs from a SpaceWire input, through the switch, to a SpaceWire output. All goals for the performance of the ASIC were achieved.

Comprehensive documentation for the SpW-10X device is available including a summary data sheet [2] and a comprehensive Users Manual [4] which allows users to understand and apply the extensive set of features in the device for their particular mission. Front line support is provided by Atmel and detailed technical support by STAR-Dundee Ltd [5].

8 Acknowledgements

9 REFERENCES

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[3] ECSS "SpaceWire Protocols", ECSS-E-ST-50-11C, Draft 1.3, July 2008

[4] C. McClements, S. Parkes, G. Kempf, "SpW-10X SpaceWire Router User Manual", Issue 3.4, July 2008 available from http://www.atmel.com/dyn/products/product_card.asp?part_id=4339

[5] http://www.star-dundee.com